

REMARKS

In the Office Action, the Examiner rejected the claims citing United States Patent Nos. 4,972,144 (Lyon et al.) and 5,289,116 (Kurita et al.).

Independent claims 1 and 9 have been amended to specifically claim that the logic circuit sequentially turns on a different single row of test structures, each time the triggering signal changes, while the other rows remain off, wherein the system is configured to sequentially test the rows of test structures, from a first row to a last row, a single row at a time each time the triggering signal changes. Applicant respectfully asserts that this is neither disclosed or suggested by the cited prior art, including Lyon et al. and Kurita et al. As such, Applicant respectfully submits that claims 1 and 9, and those claims which depend therefrom, are allowable.

The present application has been amended in response to the Examiner's Office Action to place the application in condition for allowance. Applicant, by the amendments and remarks presented above, has made a concerted effort to present claims which clearly define over the prior art of record, and thus to place this case in condition for allowance.

Should the present claims not be deemed adequate to effectively define the patentable subject matter, the Examiner is respectfully urged to call the undersigned attorney of record to discuss the claims in an effort to reach an agreement toward allowance of the present application.

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Respectfully submitted,

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